EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Exam 3

Spring 2020

Instructions: This is a take-home, open-book, open-notes exam and is due at 5:00 p.m. on Wednesday April 15. All efforts are to be individual efforts but if questions arise, please feel free to contact the instructor by email. If you prefer an oral discussion, send an email message and leave a telephone number for a return call. Please upload solutions, as a pdf file, by the due date into Canvas. There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=350\mu A/v^2$,$\mu_p C_{OX}=70\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=4fF/\mu^2$, $\lambda = 0$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF} = \infty$. Specify clearly what process parameters you are using in any solution requiring process parameters. Also attached to this exam is a table discussed in class that relates to the basic amplifier configurations.

1. (2pts) Which of the basic BJT amplifiers is characterized by a high noninverting voltage gain?

2. (2pts) The cascode configuration with MOS transistors is actually a cascade of two of the basic amplifiers. What is the first and what is the second amplifier in the cascade?

3. (2pts) How much voltage gain can be obtained from a single common emitter amplifier if ideal current sources are available for biasing?

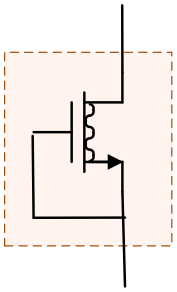
4. (2pts) How many small-signal parameters are required to characterize the small-signal model of an arbitrary nonlinear two-port network?

5. (2pts) What is the major difference between an SCR and a TRIAC?

6. (2pts) What model parameter in a JFET is analogous to the threshold voltage of a MOSFET?

7. (2pts) When using the V_{TEST}-I_{TEST} method to derive the two-port amplifier models, what termination is placed on the output port when calculating the forward voltage gain A_V?

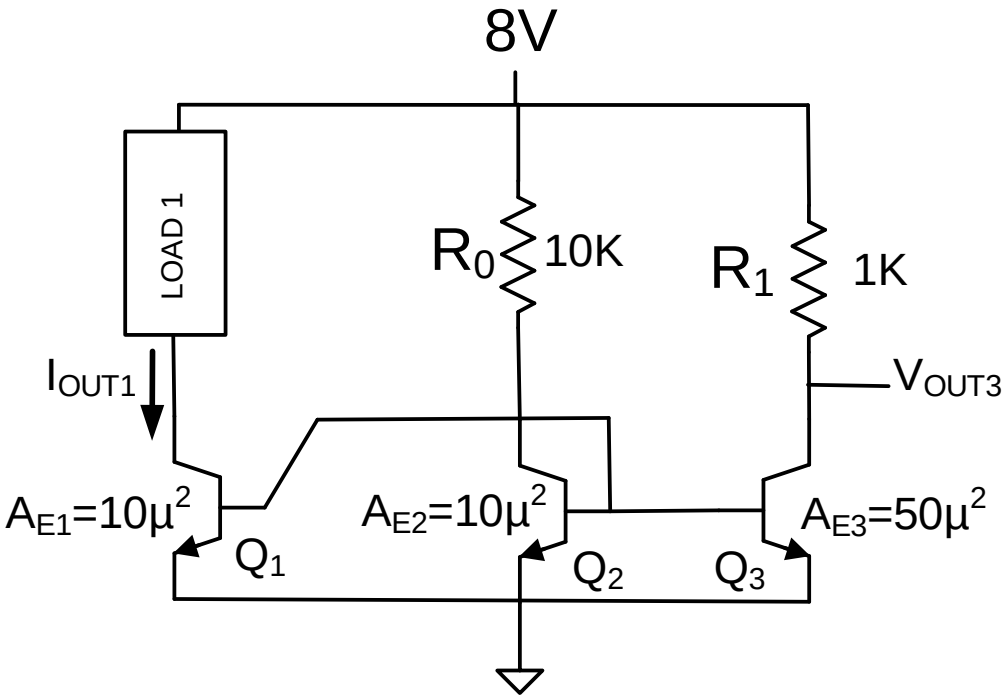
8. (2pts) Consider the small-signal schematic of the following one-port where it is assumed that the transistor is operating in the saturation region. Assume a fellow engineer argued that the small-signal equivalent circuit is an open circuit since the gate to source voltage is 0 and hence no current will flow yet previous derivations had shown that the one-port can be characterized by a resistor of value $R_{EQ} = \frac{1}{g_o}$ where g_0 is the small-signal output conductance parameter. Identify the flaw in the fellow engineer's argument.



9. (2pts) When biasing discrete amplifier circuits the current source was seldom used but the current source is widely used when biasing integrated amplifiers? What is the major reason that the current source was not a good solution when biasing discrete amplifiers yet it is often a good solution when biasing integrated amplifiers?

10. (2 pts) In the context of a two-port model for an amplifier, the term "unilateral" was used. What does it mean for an amplifier to be unilateral?

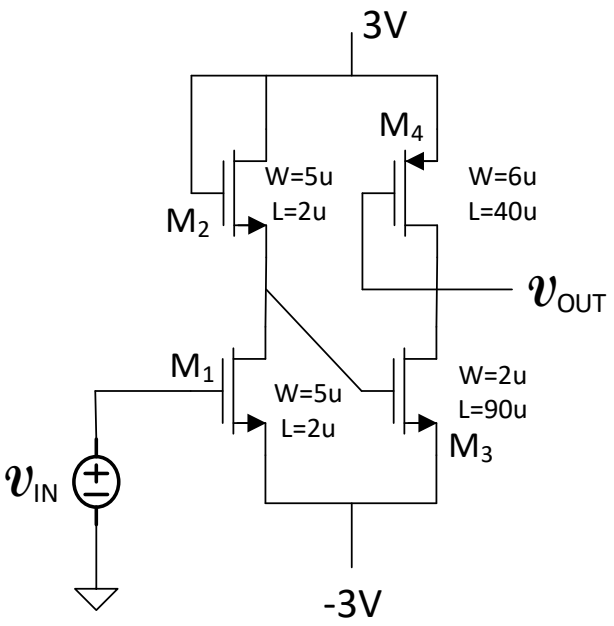
Problem 1 (16 Pts.) Consider the following circuit. Assume LOAD 1 keeps the transistor Q_1 in the forward active region and assume the β of the transistors are very large. Determine V_{OUT3} and I_{OUT1}.



Problem 2 (16 Pts.) Consider the following amplifier.

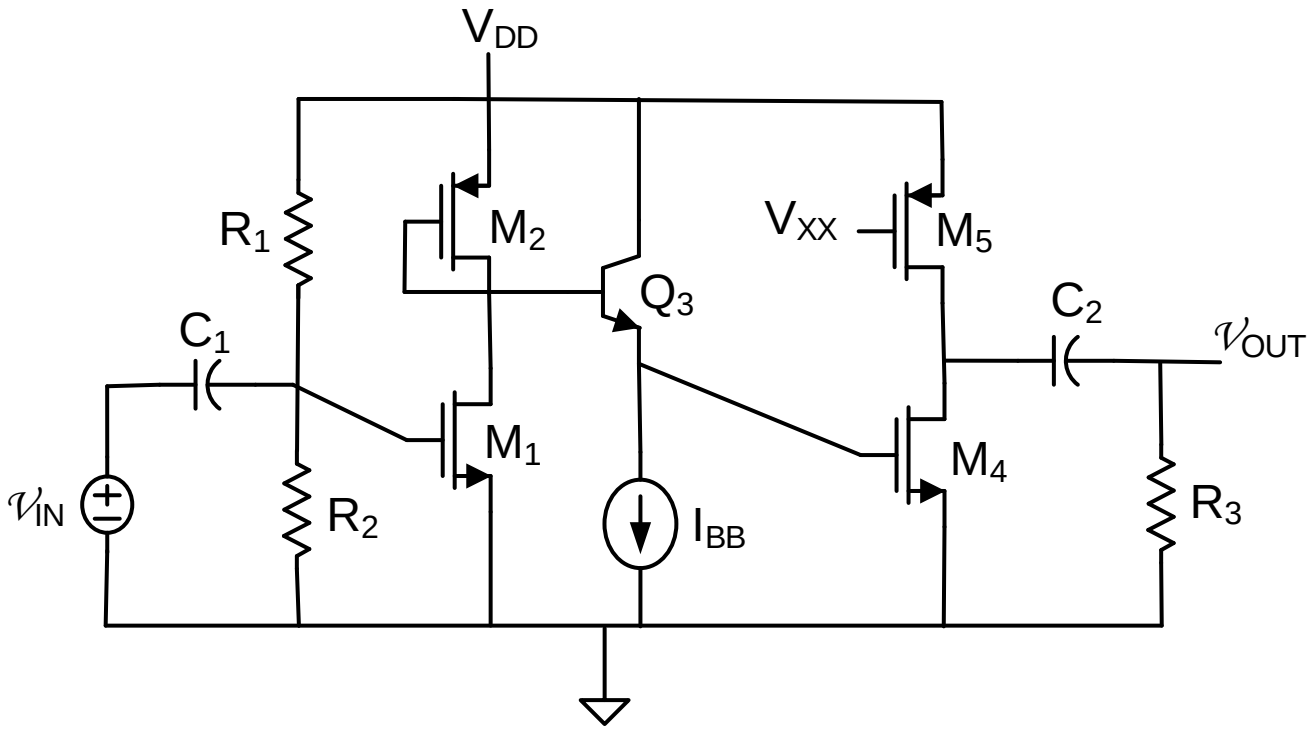
a) Assuming the transistors are all operating in the saturation region, derive the small signal gain in terms of the small signal model parameters

b) Numerically determine the voltage gain for the circuit.



Problem 3 (16 Pts.) Consider the following circuit. Assume the DC current source I_{BB}, the voltage source V_{XX}, and the biasing resistors have all been chosen so that the MOS transistors are operating in the saturation region and the BJT is operating in the forward active region. Assume also that the capacitors C_1 and C_2 are large.

a) Draw the small signal equivalent circuit
b) Determine the small-signal voltage gain in terms of the small-signal model parameters

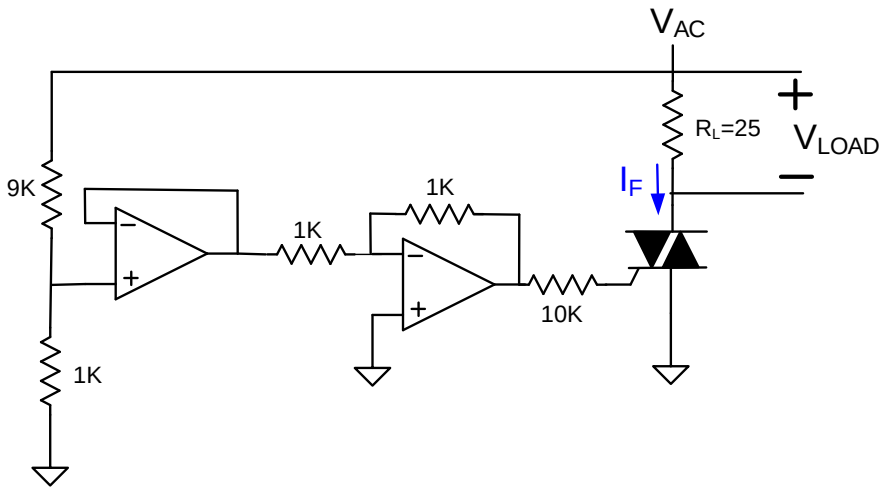


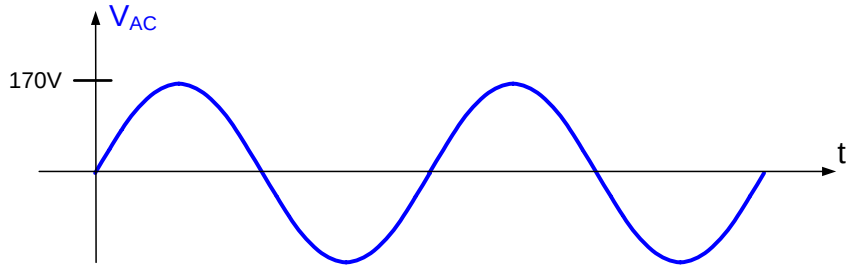
Problem 4 (16 Pts.) Design a voltage amplifier that has a gain of $A_V = -3$ using MOS transistors, a single 2V DC power supply, and any number of resistors and capacitors. Clearly indicate the size of the transistors and the values for all passive components. Include any biasing that is required for your amplifier.

Problem 5 (16 Pts) Consider the following circuit. Assume the op amps are ideal, the magnitude of the gate trigger voltage of the Triac is 2V, and the gate trigger current is small. The waveforms V_{AC} is the standard 60Hz line voltage shown below.

a) (12pts) Obtain an expression for and plot $V_{LOAD}(t)$ for one period of the excitation

b) (4 pts) Determine the quadrants of operation of the Triac





MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

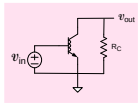
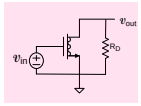
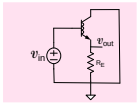
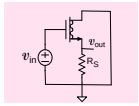
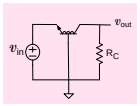
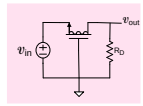
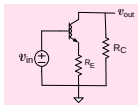
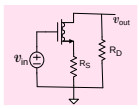
CAPACITANCE PARAMETERS

	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

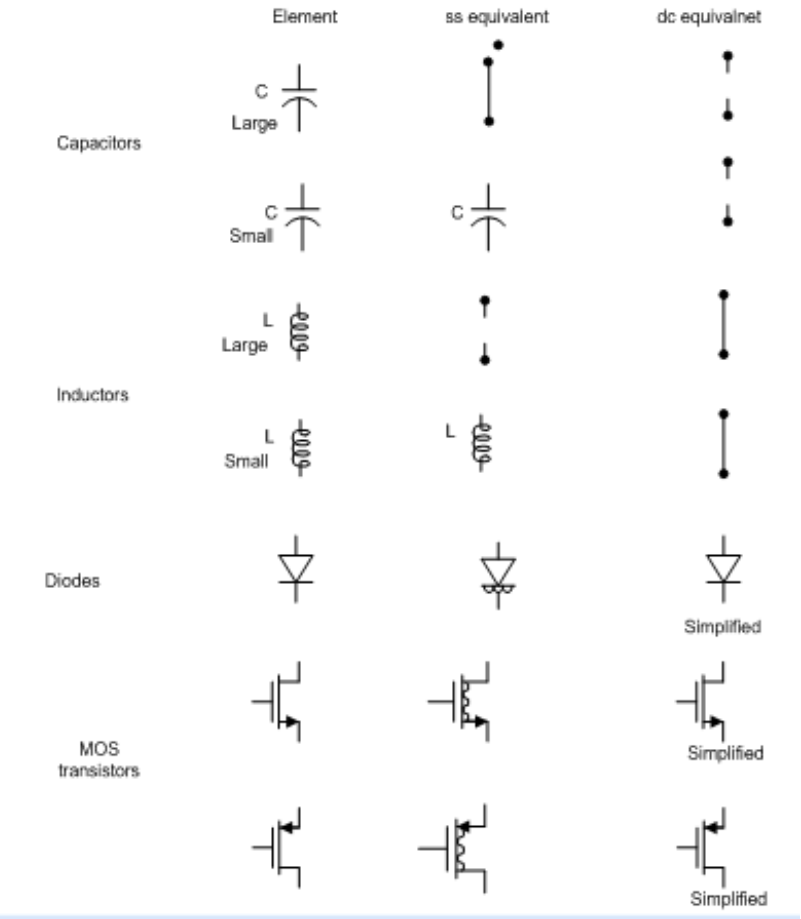
COMMENTS: DEEP_SUBMICRON

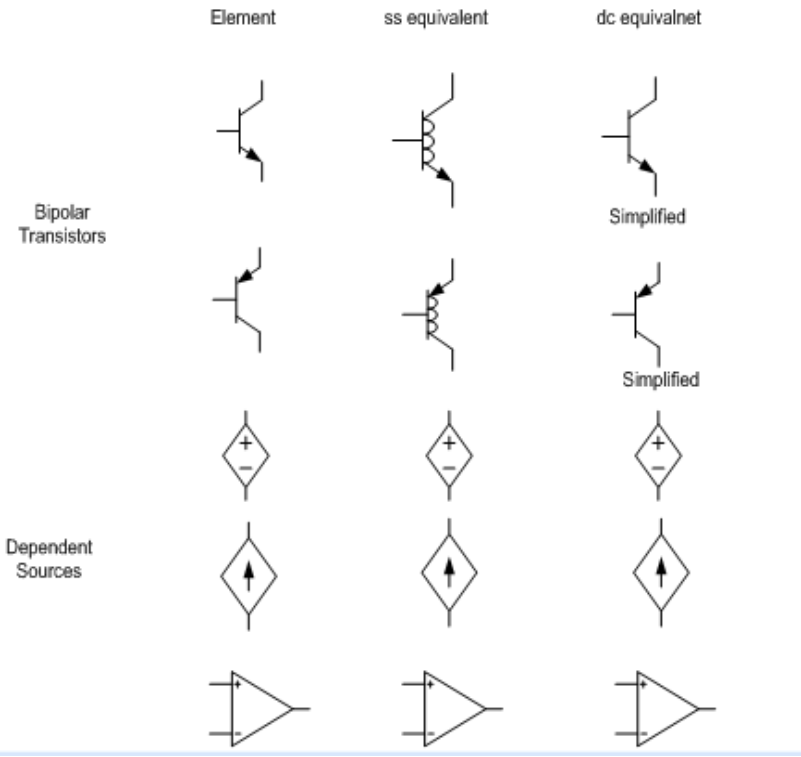
Basic Amplifier Gain Table

	CE/CS		CC/CD		CB/CG		CEwRE/CSwRS	
	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
								
A_V	$-g_mR_C$		$\frac{g_m}{g_m+g_E} \simeq 1$		g_mR_C		$-\frac{R_C}{R_E}$	
	$-\frac{I_{CQ}R_C}{V_t}$	$-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$	$\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	$\frac{I_{CQ}R_C}{V_t}$	$\frac{2I_{DQ}R_C}{V_{EB}}$		
R_{in}	r_π		$r_\pi + \beta R_E$		g_m^{-1}		$r_\pi + \beta R_E$	
	$\frac{\beta V_t}{I_{CQ}}$	∞	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞	$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞
R_{out}	R_C		g_m^{-1}		R_C		R_C	
			$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$				

Dc and small-signal equivalent elements

	Element	ss equivalent	dc equivalnet
dc Voltage Source	V_{DC}		V_{DC}
ac Voltage Source	V_{AC}	V_{AC}	
dc Current Source	I_{DC}		I_{DC}
ac Current Source	I_{AC}	I_{AC}	
Resistor	R	R	R


Element
ss equivalent
dc equivalnet
Capacitors
C
Large
C
Small
C
Inductors
L
Large
L
Small
L
Diodes
Simplified
MOS
transistors
Simplified
Simplified


Element
ss equivalent
dc equivalnet
Bipolar
Transistors
Simplified
Simplified
Dependent
Sources